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## NOTICE OF ALLOWANCE AND FEE(S) DUE

54406

7590

08/29/2008

AKA CHAN LLP / CISCO 900 LAFAYETTE STREET SUITE 710 SANTA CLARA, CA 95050

EXAMINER				
CHEA, PHILIP J				
ART UNIT PAPER NUMBER				

2153 DATE MAILED: 08/29/2008

	APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
Ī	09/909,049	07/18/2001	Suresh Katukam	CISCP694	8487

TITLE OF INVENTION: METHOD AND APPARATUS FOR COMPUTING A PATH IN A SYSTEM WITH NODAL AND LINK DIVERSE

CONSTRAINTS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1440	\$0	\$0	\$1440	12/01/2008

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

#### HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

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B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

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B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

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SANTA CLARA	A, CA 95050		ſ						(Depositor's name)
									(Signature)
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APPLICATION NO.	FILING DATE		FIRST NAMED INVENT	ГOR		ATTO:	RNEY DOCKET NO.	CONFI	RMATION NO.
09/909,049	07/18/2001	•	Suresh Katukam				CISCP694		8487
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nonprovisional	NO	\$1440	\$0		\$0		\$1440		12/01/2008
EXAM	INER	ART UNIT	CLASS-SUBCLASS						
CHEA, P	PHILIP J	2153	709-239000						
Change of correspondence address or indication of "Fee Address" (37 FR 1.363).  Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.  "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.			(1) the names of up or agents OR, altern (2) the name of a single registered attorney	a single firm (having as a member a new or agent) and the names of up to ent attorneys or agents. If no name is					
PLEASE NOTE: Unle	ess an assignee is identi h in 37 CFR 3.11. Comp	A TO BE PRINTED ON The fied below, no assignee eletion of this form is NO	data will appear on th	ne par g an a	tent. If an assigne ssignment.			ocument l	has been filed for
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900 LAFAYETTI	E STREET		ART UNIT	PAPER NUMBER		
SUITE 710 SANTA CLARA,	CA 95050		2153 DATE MAILED: 08/29/200	8		

# **Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)**

(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 548 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 548 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

	Application No.	Applicant(s)		
	09/909.049	KATUKAM ET AL.		
Notice of Allowability	Examiner	Art Unit		
	DUILID I CHEA	2152		
	PHILIP J. CHEA	2153		
The MAILING DATE of this communication apperature All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RI of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in thi or other appropriate communic GHTS. This application is subj	s application. If not included ation will be mailed in due course. <b>THIS</b>		
1. X This communication is responsive to <u>communication filed A</u>	April 3, 2008.			
2. $\boxtimes$ The allowed claim(s) is/are $\underline{1,8-11,19-21,37,38,46}$ and $\underline{47}$ .				
<ul> <li>3. ☐ Acknowledgment is made of a claim for foreign priority ur</li> <li>a) ☐ All b) ☐ Some* c) ☐ None of the:</li> <li>1. ☐ Certified copies of the priority documents have</li> <li>2. ☐ Certified copies of the priority documents have</li> </ul>	been received.			
3. ☐ Copies of the certified copies of the priority do				
International Bureau (PCT Rule 17.2(a)).		3 11		
* Certified copies not received:				
Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDONN THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.		eply complying with the requirements		
4. A SUBSTITUTE OATH OR DECLARATION must be subm INFORMAL PATENT APPLICATION (PTO-152) which give				
5. CORRECTED DRAWINGS ( as "replacement sheets") mus	st be submitted.			
(a) $\square$ including changes required by the Notice of Draftspers	on's Patent Drawing Review (F	PTO-948) attached		
1) 🔲 hereto or 2) 🔲 to Paper No./Mail Date				
(b) ☐ including changes required by the attached Examiner's Paper No./Mail Date	s Amendment / Comment or in t	the Office action of		
Identifying indicia such as the application number (see 37 CFR 1 each sheet. Replacement sheet(s) should be labeled as such in t				
6. DEPOSIT OF and/or INFORMATION about the depo attached Examiner's comment regarding REQUIREMENT				
Attachment(s) 1. ☐ Notice of References Cited (PTO-892)	5 Notice of Inform	nal Patent Application		
Notice of Neterences Great (1 10-092)     Notice of Draftperson's Patent Drawing Review (PTO-948)	6. ☐ Interview Sumr	• •		
	Paper No./Mai	il Date		
3. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date	7. 🛛 Examiner's Am	enamentComment		
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material  8. ☑ Examiner's Statement of Reasons for Allowance				
District Observation	9.			
Philip J Chea Examiner				
Art Unit: 2153				

#### **EXAMINER'S AMENDMENT**

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Gary Aka 29,038 on August 26, 2008.

The application has been amended as follows:

### IN THE CLAIMS:

Please see attached.

2. The following is an examiner's statement of reasons for allowance: The prior art does not teach nor render obvious each and every limitation of the claimed invention. Specifically, the prior art fails to teach the particulars of selectively generating a nodal diverse alternate circuit path by inputting nodal and link diverse constraints and generating the primary circuit path that includes the first element and a set of elements selected from the plurality of elements, and identifying the first element and the set of elements as being inaccessible for use in subsequently generating the alternate circuit path.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHILIP J. CHEA whose telephone number is (571)272-3951. The examiner can normally be reached on M-F 6:30-4:00 (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glenn Burgess can be reached on 571-272-3949. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Glenton B. Burgess/ Supervisory Patent Examiner, Art Unit 2153 Philip J Chea Examiner Art Unit 2153

PJC 8/26/08

Art Unit: 2153

Claim 1 (currently amended): A device for computing circuit paths between a first node and a second node within a network, the network including a plurality of elements which includes a protected link, the device comprising:

a memory;

a route generator, the route generator being arranged to generate a primary circuit path between the first node and the second node, the primary circuit path including a first element <u>and a set of elements</u> selected from the plurality of elements, wherein the route generator is configurable to selectively generate a nodal diverse alternate circuit path when a nodal diverse constraint is input and a link diverse alternate circuit path when a link diverse constraint is input further being arranged to specify circuit characteristics for the primary circuit path and for the alternate circuit path; and

a list mechanism, the list mechanism being stored in the memory, the list mechanism being arranged to identify the first element, wherein the route generator is further arranged to generate an alternate circuit path between the first node and the second node using the list mechanism and the input, the list mechanism being arranged to identify the first element, the set of elements and the protected link as being inaccessible for use in subsequently generating the alternate circuit path, wherein the alternate circuit path does not include the first element, the set of elements and the protected link identified by the list mechanism.

Claims 2-7 (canceled)

Claim 8 (previously presented): A device as recited in claim 1 wherein when the nodal diverse constraint is input, the first element is a node.

Claim 9 (previously presented): A device as recited in claim 1 wherein when the link diverse constraint is input, the first element is a link.

Claim 10 (original): A device as recited in claim 1 wherein the device is associated with the first node.

Claim 11 (original): A device as recited in claim 1 wherein the route generator is further arranged to implement the primary circuit path and the alternate circuit path.

Claims 12-18 (canceled)

Claim 19 (currently amended): An element for use in an optical network, the optical network including a plurality of nodes, the plurality of nodes including a destination node, the optical network further including a plurality of links, the element comprising:

a memory;

a route generator, the route generator being arranged to compute a first circuit path between the element and the destination node, the first circuit path including a first link included in the plurality of links <u>and further arranged to identify the first link and to generate a first identifier that identifies the first link, wherein the route generator is configurable to selectively generate a nodal diverse alternate circuit path when a nodal diverse constraint is input and a link diverse alternate circuit path when a link diverse constraint is input, the input further being arranged to specify circuit characteristics for the first circuit path and for the second circuit path; and</u>

a list, the list being stored in the memory, the list including a plurality of identifiers, the plurality of identifiers being arranged to identify selected links included in the plurality of links, the plurality of

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identifiers including a the first identifier that identifies the first link, wherein the route generator is further arranged to place the first identifier in the list and to generate the plurality of identifiers that are arranged to identify the selected links and to place the plurality of identifiers in the list, and is further arranged to compute the second circuit path using the list and the input, wherein the second circuit path includes a second link included in the plurality of links and does not include the selected links identified by the plurality of identifiers included in the list, wherein a failure of any of the selected links identified by the plurality of identifiers included in the list does not affect computing of the second circuit path.

Claim 20 (original): An element according to claim 19 wherein the selected links included in the plurality of links include a protected link.

Claim 21 (original): An element according to claim 19 wherein the element is a source node.

Claim 22-36 (canceled)

Claim 37 (previously presented): The device of claim 1 wherein the route generator is arranged to generate the primary circuit path and the alternate circuit path as nodal diverse paths in which the primary circuit path and the alternate circuit path have no common nodes between the first node and the second node, and wherein when the primary circuit path and the alternate circuit path are the nodal diverse paths, the first element is a node.

Claim 38 (previously presented): The device of claim 1 wherein the route generator is arranged to generate the primary circuit path and the alternate circuit path as link diverse circuit paths in which the primary circuit path and the alternate circuit path share no links between the first node and the second node, and wherein when the primary circuit path and the alternate circuit path are the link diverse circuit paths, the first element is a link.

Claim 39-45 (canceled)

Claim 46 (previously presented): A device as recited in claim 1 wherein the nodal diverse constraint specifies that any nodes in the primary circuit path between the first node and the second node are not included in the alternate circuit path and wherein the link diverse constraint specifies that any links in the primary circuit path between the first node and the second node are not included in the alternate circuit path.

Claim 47 (previously present): The device of claim 1 wherein the circuit characteristics include a load characteristic.